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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,818	11/29/2001	Eiji Furukawa	122.1476	9741

21171 7590 09/21/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
ROSARIO-VASQUEZ, DENNIS	
ART UNIT	**PAPER NUMBER**
2621	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,818	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Dennis Rosario-Vasquez	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/29/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaiser et al. (US Patent 4,970,664 A).

Regarding claim 1, Kaiser et al. discloses a logic drawing entry apparatus (" computer" in col. 3, line 35) comprising

a) a means ("schematic editor" in col. 3, lines 35,36) for creating an inter-drawing connection diagram file (Fig. 1 shows multiple schematic diagrams created from a designer and inter-connected with associated files names, ADD-DET SHEET 1 and DECODE SHEET 1 as mentioned in col. 3, lines 43-57.) which describes relations of mutual connections between a plurality of drawings (The drawings of fig. 1 as also shown in fig. 2, num. 18a-18c that are interconnected.), and

b) an inter-drawing connection indication means (Fig. 2, num. 10:"display" as mentioned in col. 4, line 17) which indicates, on one screen (fig. 2, num. 16), a plurality of the drawings (fig. 2, num. 18a-18c) outlined (fig. 2, num. 20a and 20b are separators that create a division between schematic sheets 18a-18c.) according to the description (The filename, ADD-DET SHEET 1 with the associated schematic diagram of figure 1 is shown in figure 2, num. 18a as mentioned in col. 4, lines 48-53.) in the inter-drawing connection diagram file (Fig. 1 shows multiple schematic diagrams connected with associated files names, ADD-DET SHEET 1 and DECODE SHEET 1 , as mentioned in col. 3, lines 43-57.) which has been created (by the designer).

Regarding claim 2, Kaiser et al. discloses the logic drawing entry apparatus (" computer" in col. 3, line 35) of claim 1 further comprising an inter-drawing connection diagram editing means ("source code" in Appendix A and mentioned in col. 6, line 13 generates a diagram 10 using connectivity and editing functions of creating a new window to draw in, starting point for a drawing and terminating a line from a drawing as mentioned in col. 6, lines 12-25.) for implementing editing works (fig. 1 are created from a schematic editor.) on each of a plurality of said drawings (fig. 2, num. 18a-18c) when a plurality of said drawings are indicated on one screen (The drawings of fig. 2, numerals 18a-18d or 16 is shown in it's entirety "within the path context window 16 (col. 5, lines 35-37)."

Claim 3 has been addressed in claim 2.

Regarding claim 4, Kaiser discloses the logic drawing entry apparatus (" computer" in col. 3, line 35) of claim 2 wherein said inter-drawing connection diagram editing means ("source code" in Appendix A generates a diagram 10 using connectivity and editing functions of creating a new window to draw in, starting point for a drawing and terminating a line from a drawing as mentioned in col. 6, lines 12-25.) has a function ("hllite" in col. 6, line 55.) of modifying the attributes ("indicia" are highlighted as mentioned in col. 6, lines 55-57) of each drawing (Fig. 2, num. 16 is a window of drawings or objects that will be highlighted as mentioned in col. 6, lines 55-57.) on an indication screen (Fig. 2, num. 10 is a display screen.).

Regarding claim 5, Kaiser et al. discloses the logic drawing entry apparatus ("computer" in col. 3, line 35) of claim 1 further comprising

a) an inter-drawing connection counting means (fig. 4, num. 38:CONNECTIVITY STRUCTURE describes "the instances and nets connected to each pin (col. 7, lines 16-18).") for counting the number of connections (fig. 4, num. 38:CONNECTIVITY STRUCTURE provides data that includes the number of instances or symbols with associated nets or lines between each instant for a window 16 of fig. 2 as mentioned in col. 5, lines 30-40.) between a plurality of said drawings (fig. 2, numerals 18a-18c or num. 16) about symbols (Figure 2, num. 16 has symbols or instances as shown in num. 16) included in a plurality of said drawings (fig. 2, numerals 18a-18c or num. 16), and

b) a net connection relation drawing means (Fig. 4, num. 46:DISPLAY GENERATOR for drawing the window 16 of fig. 2 as mentioned in col. 7, lines 10-12.) for drawing net connection relations between said drawings (fig. 2, numerals 18a-18c or num. 16) based (Fig. 4, num. 46:DISPLAY GENERATOR receives data from fig. 4, num. 38 to draw the window 16 of fig. 2) on the number of inter-drawing connections counted by said inter-drawing connection counting means (fig. 4, num. 38:CONNECTIVITY STRUCTURE provides data that includes the number of instances or symbols with associated nets or lines between each instant for a window 16 of fig. 2 as mentioned in col. 5, lines 30-40.).

Regarding claim 6, Kaiser et al. discloses the logic drawing entry apparatus of claim 5 wherein said net connection relation drawing means (Fig. 4, num. 46:DISPLAY GENERATOR for drawing the window 16 of fig. 2 as mentioned in col. 7, lines 10-12.) has a function of modifying the indications of the nets (Fig. 4, num. 46 draws highlighted nets in a window that is generated based on data from fig. 4, num. 36 as mentioned in col. 7, lines 33-35 and 41,42.) according to said number of inter-drawing connections (fig. 4, num. 38:CONNECTIVITY STRUCTURE provides data that includes the number of instances or symbols with associated nets or lines between each instant for a window 16 of fig. 2 as mentioned in col. 5, lines 30-40.)..

Regarding claim 7, Kaiser et al. discloses the logic drawing entry apparatus of claim 1 further comprising

a) a drawing name modifying means ("drawSheetBoundary" in col. 8, line 11.) for modifying ("Sheet identifiers or labels are generated" from the sheets of fig. 1 as mentioned in col. 8, lines 10-15 using drawSheetBoundary.) the names (filenames of the sheets in fig. 1) of a plurality of said drawings (Fig. 1 has a plurality of drawings or sheets.), and

b) a drawing name arranging means("drawSheetBoundary" in col. 8, line 11. has a separator means in addition to the sheet identifier means above as mentioned in col. 8, lines 10-15.) for arranging said drawings(The drawings of fig. 1 are also shown in fig. 2, num.18a-18c) in ascending or descending order (Fig. 2, num. 20a is the separator with down arrows that descends to a lower design level as mentioned in col. 4, line 65-67.) based on the modified drawing names (The sheet identifier indicates sheet 1 of file name DECODE of fig. 1, which is the lower design level as mentioned from col. 4, line 67 to col. 5, line 4.).

Regarding claim 8, Kaiser et al. discloses the logic drawing entry apparatus of claim 7, wherein said drawing name arranging means ("drawSheetBoundary" in col. 8, line 11. has a separator means in addition to the sheet identifier means above as mentioned in col. 8, lines 10-15.) has a function (fig. 2:separator 20a and 20b) of designating intervals (Separators separate the drawings 18a-18c) between drawings.

Regarding claim 14, Kaiser et al. discloses a logic drawing entry apparatus for processing of drawings in which hierarchic symbols having a plurality of pins are described, the logic drawing entry apparatus comprising

a) a hierarchic symbol drawing means (Fig 4., num. 36:GRAPHICS STRUCTURE contains symbols with rectangular symbols and progressively detailed layers from the top rectangle to the lower rectangle as shown in figure 1.) for drawing individual symbols (Fig. 4, num. 36 has symbols that correspond to circuit components.) constituting said hierarchic symbols (The lower detail layers of figure 1.), and

b) a net drawing means (Fig. 4, num. 46:DISPLAY GENERATOR) for drawing nets (Fig. 4, num. 36 has nets as shown by the lines between circuit components 1-3.) for individual symbols (components 1-3) which have been drawn (The circuits of fig. 4, num. 36 were initially designed.).

4. Claims 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Mankin et al. (US Patent 5,625,567 A).

Regarding claim 9, Mankin et al. discloses a logic drawing entry apparatus for processing of drawings in which a plurality of symbols, and nets expressing connection relations between symbols, are indicated, the logic drawing entry apparatus comprising

a) a symbol selecting means (A user selects a "package" as mentioned in col. 6, lines 1-3 and shown in fig. 5, num. 30:SET UP TECHNOLOGY AND UTILIZATION OF COMPONENTS,PINS, AND REGISTERS.) for selecting symbols (Fig. 14, numerals 191 and 193 are symbols selected from the above package.) to be moved and positions (Fig. 15 shows the same components moved relative to the

positions of the components shown in fig. 14 of to another position.) where the selected symbols (Fig. 14, numerals 191 and193) are moved (As shown in fig. 15.),

b) a symbol moving means (A user interactively moves the symbols with a computer and shown in step 36 of fig. 5 as mentioned in col. 5, lines 39-42.) for moving said selected symbols to said positions (Fig. 15 corresponds to the step of moving in fig. 5, step 36.),

c) a symbol replacing means (A program with a triggering instruction that replaces components as mentioned in col. 11, lines 17-39 as shown in fig. 9, num. 86:SUBSTITUTE TERMINAL LOGIC) for replacing positions (Fig 14 has components 191 and 193 positioned as shown to be replaced.) of said selected symbols (Fig. 14, numerals 191 and 193 are symbols selected from the above package.) with the positions (Fig. 15 has the a component 194 that replaced components 191 and 193 of fig. 14 based upon a triggering instructions as mentioned in col. 11, lines 36-39.) where said selected symbols are (fig. 15, numerals 198 and 196 are the repositioned symbols moved from the positions shown in fig. 14, numerals 191 and 193.) when other symbols (PARTION OUTPUT of fig. 14) than said selected symbols (Fig. 14, num. 191 and 193) exist (PARTION OUTPUT of fig. 14 is required to trigger a replacement as mentioned in col. 11, lines 31-33.) at the positions (The symbol PARTION OUTPUT exists at the output of component 193.) where said selected symbols (fig. 14, num. 191 and 193) are moved (The PARTION OUTPUT shown labeled as "0" in fig. 15 is still attached to the component 193 renumbered as 198 and reduced in size as compared to PARTION OUTPUT of fig. 14.) where the selected components are moved (The selected

components 191 and 193 renumbered 198 and 196 in fig. 15 partially cover the symbol PARTITION OUTPUT of fig. 14 as shown in fig. 15), and

d) a net redrawing means (Fig. 9, step 88:WRITE OUT INTERNAL COMPONENT INSTANCES) for redrawing nets for said selected symbols after the movement or replacement (Mankin et al. states, "After the system recognizes and substitutes terminal logic, it writes out internal component instances of the resulting design and the connected nets of each components in step 88 (FIG. 9) (col. 11, lines 40-43).") while keeping the connection relations between said selected symbols before the movement (Fig.15 maintains the same connection relations before movement of the connection relations shown in fig. 14.).

Claim 10 has been addressed in claim 9.

Regarding claim 11, Mankin et al. discloses the logic drawing entry apparatus of claim 9 further comprising an arranging means ("net list" in col. 6, line 53) for arranging a plurality of selected symbols (The net list wires symbols together as mentioned in col. 6, lines 53-57) on a drawing in a vertical line or a horizontal line (Fig. 14 shows a plurality of symbols arranged or wired as shown as horizontal lines.).

Regarding claim 12, fig. 14 shows line intervals designated with letters T, I and O.

Claim 13 has been addressed in claim 9.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamamoto et al. (US Patent 5,159,664 A) is pertinent as teaching a method of selecting an object for moving the object to a new position as shown in fig. 4.

IBM Technical Disclosure Bulletin, Vol. 36, Issue 11, pages 615-616 is pertinent as teach a method of using a replace window that substitutes a set of components A,B and N1 for one component C.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis Rosario-Vasquez whose telephone number is 703-305-5431. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DRV
Dennis Rosario-Vasquez
Unit 2621

LEO BOUDREAU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600